21/4/12 (Gato 10:00)

Power Ele

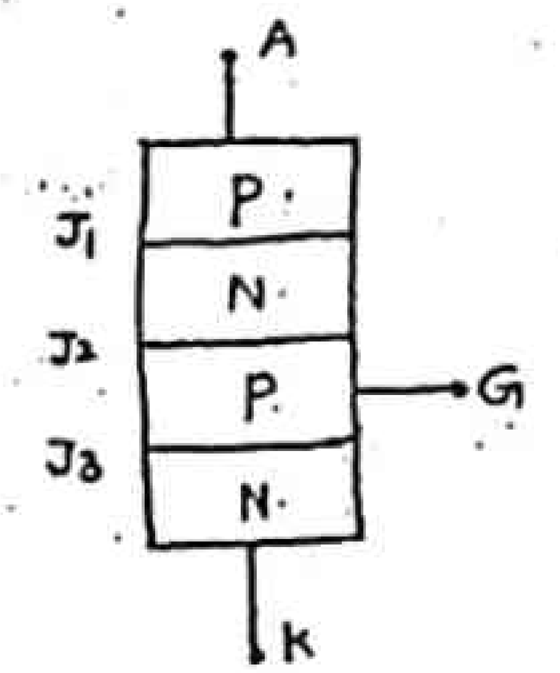
* "Diode" is a "Uncontrolled" Device. "Thyristor" is a "Controlled" device where the instant of Conduction can be Controlled after applying the forward Voltage

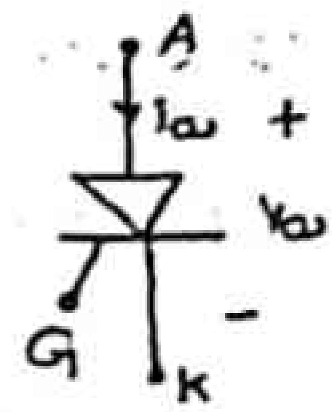
* Due to this Control. o/p Voltage, current and power may be Controlled.

* "Thyristor" is the name given to the "family" of devices and having a Common Structure "pnpn" and they will be useful in power Control Applications.

* "SCR" is the first "member" of "thyristor" family

SCR:



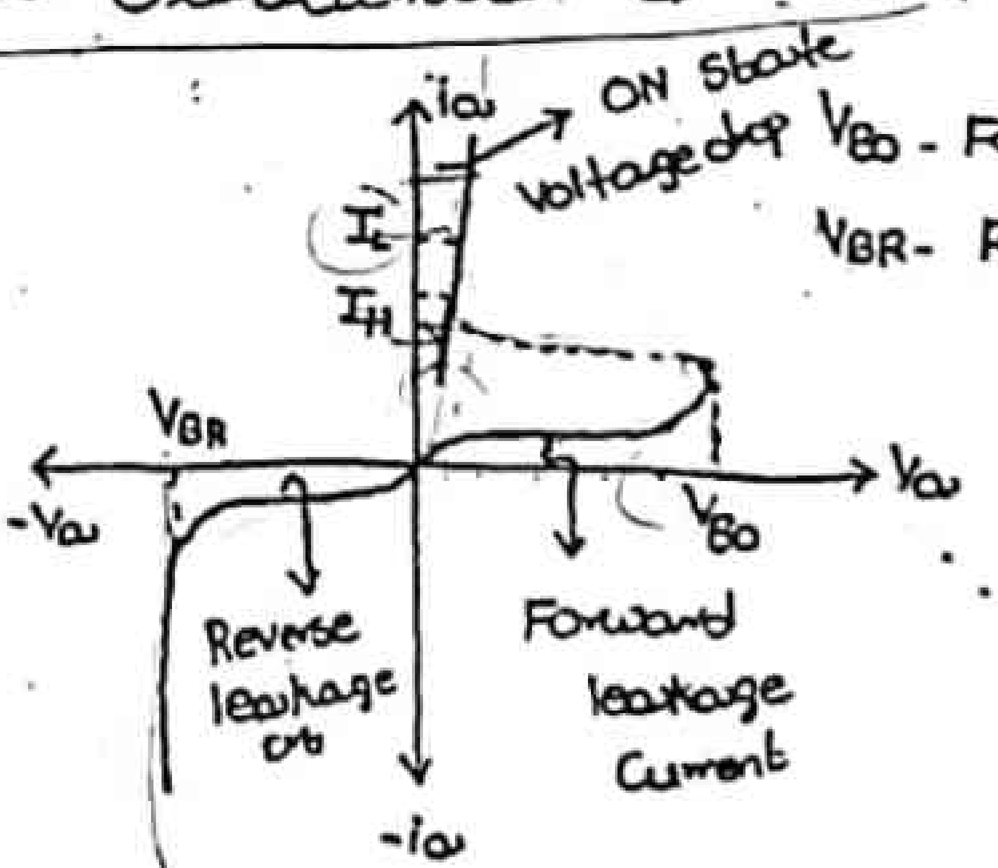


* External P-layer Terminal - Anode
* Internal P-layer Terminal - Gate
* Outer N-layer Terminal - Cathode

} Four layered Three Junction device

* SCR is a 4 layered, three Junction, three terminal pnpn device

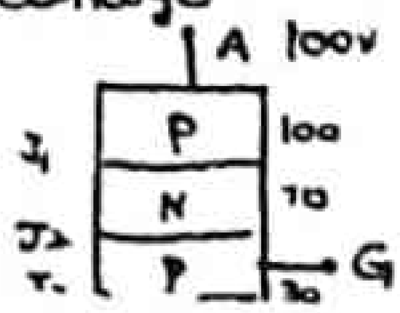
Static Characteristics of SCRS:



V_{BO} - Forward Break over Voltage

V_{BR} - Reverse Break over Voltage

* In the fwd blocking state, J_1, J_3 are fwd biased J_2 will be reverse biased. only leakage Current flows i.e, fwd leakage Current



J_2 reverse biased as

... N

* In the "Fwd blocking State," SCR is equivalent to "open Switch" ("Voltage" across the device is Same as the "Supply Voltage" and "Current" is "Fwd leakage Current." (Assume to be 0)

I=0
V=Vs

1) Forward Voltage Triggering:-

* In this method, a high fwd Voltage will be applied due to which Reverse biased Junction "J_2" break down, SCR Starts Conduction.

* The Amount of fwd Voltage reqd to turn on the SCR (without gate pulse) is known as Forward breakover Voltage. "Avalanche Break down"

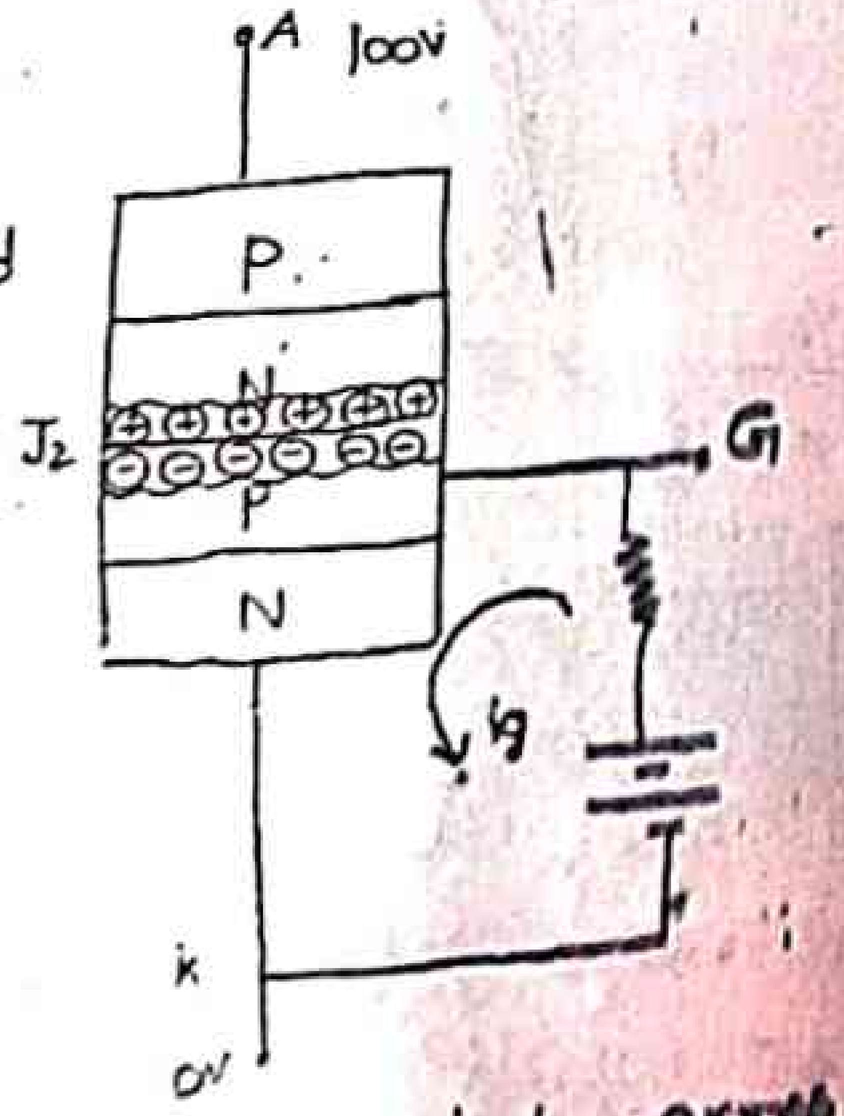
- "Turn on" of SCR - "Fwd Blocking State" to "Fwd Conduction State"
- "Turn Off" of SCR - "Fwd Conduction State" to "Fwd Blocking State"

In the fwd Conduction state, SCR is equivalent to "Forward closed Switch. The "Voltage" across the device is "load Voltage drop" and "Current" through the device is "load Current."

* It is a method to turn on the SCR but not a practical method bcz it needs a high Voltage

2) Gate Triggering:-

J_2 is Reverse biased and Contains Some depletion layer (Immobile ions (no Charge Carriers))

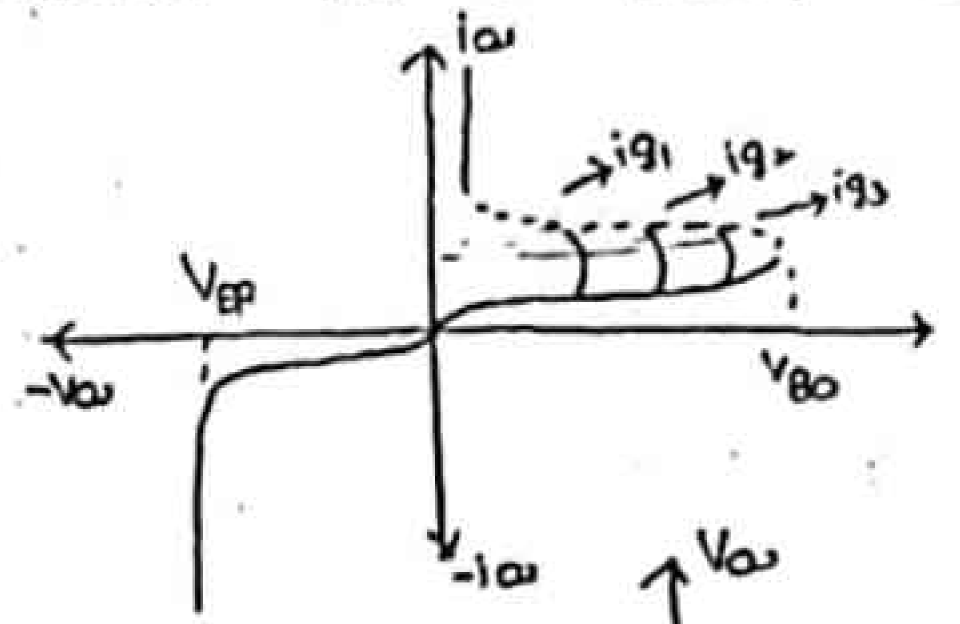


Ig - due to movement of charge Carriers

Some move depletion layer and recombination takes place

* A fwd Voltage will be applied across Gate to Cathode ... The

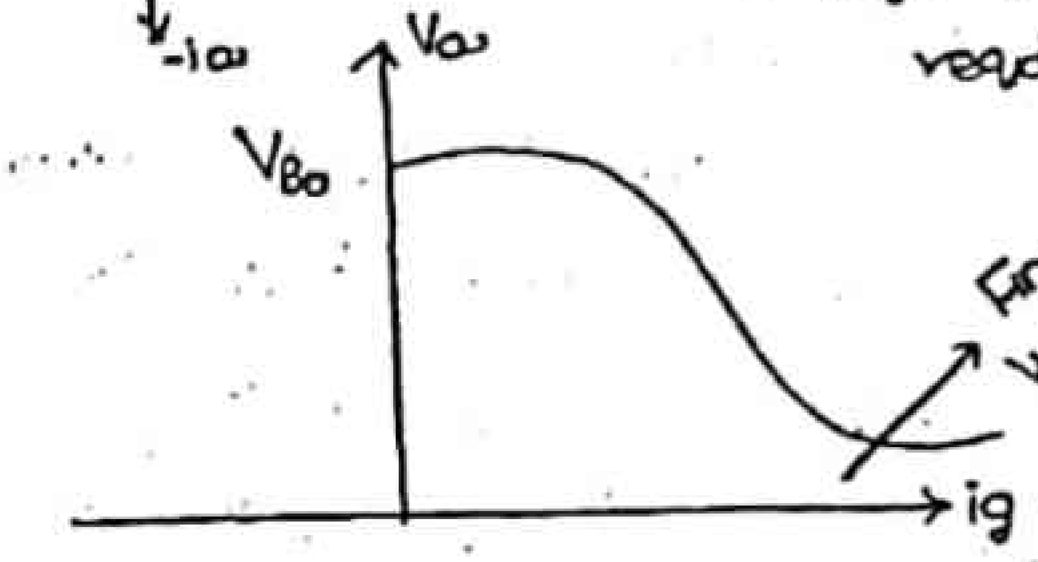
Current is due to movement of charge carriers. Then recombinations will be taking place in depletion layer due to availability of charge carriers. Hence, width of depletion layer decreases. As a result, SCR starts conduction



$ig_1 > ig_2 > ig_3$

Zero gate Current – high voltage reqd to turn on SCR

* High gate Current - less Voltage reqd to turn on SCR



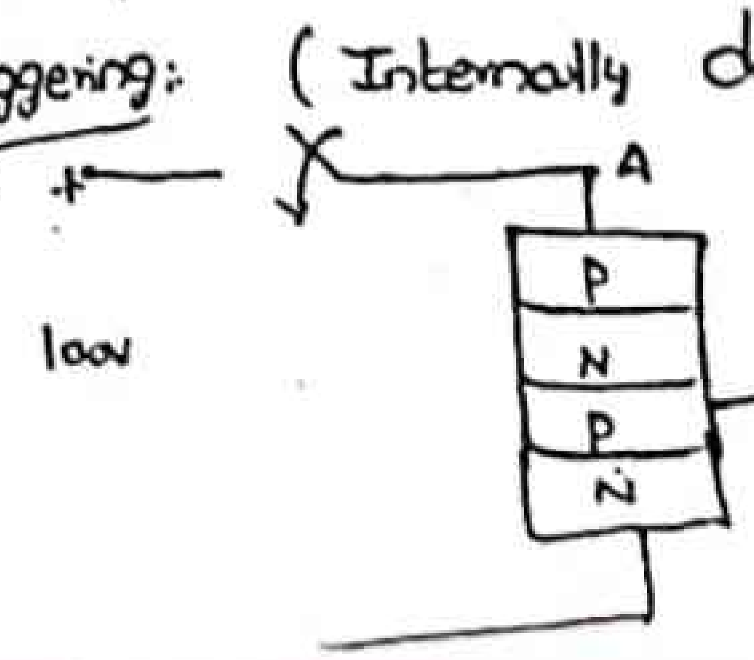
High gate current Anode Voltage to turn on SCR decreases

* By employing the "higher Values" of the gate Currents, the "Anode Voltage" reqd to "turn on" the "SCR decreases"
* A "Min. Frwd Voltage" reqd to "turn on SCR" for any gate value of Current and it is known as "Finger Voltage"
* Great advantage of Gate triggering allows to turn on SCR for a Range of Voltages by applying appropriate gate Currents.

③ Thermal Triggering: In this method, SCR will be heated up due to which energy levels of charge carriers will be Increased, as a result we are able to cross the Junction and allow the Conduction.

④ Light Triggering: An Intensified light beam focused on SCR due to which energy levels of charge carriers Increases. Hence, the device starts Conduction

⑤ dv/dt triggering: (Internally developed Mechanism)



$V_1 = 0$ (Before closing switch)

$V_2 = 100V$

$dt = 1ms$ (time to develop

$C_J = 1\,\mu F$; $I = C_J \frac{dv}{dt}$ (Charging Current)

$= 1\times10^{-6}\frac{(100-0)}{1\times10^{-3}} = 0.1\,A$

If Charging Current is more than rated gate Current of SCR, SCR Conducts

* While applying the forward Voltage, the Junction cap. will be Subjected to rate of change of Voltage (dv/dt), it results into a Charging Current $\left[I = C\frac{dv}{dt}\right]$. If the Value of charging current more than rated gate Current of SCR, then it Starts Conduction. This method is known as (dv/dt) triggering

* No Control (Control is lost) after applying the Fwd voltage (As Gate is not involved)

If we want to avoid (dv/dt) triggering, dv/dt should be low

* Due to lack of Control Action, $\left(\frac{dv}{dt}\right)$ triggering is to be avoided. It is possible by making lower Value of (dv/dt)

* Out of all methods, Gate triggering is preferable

Latching Ct: It is associated with turn on process. It is the min. Value of Ct above which anode Current Should rise for the reliable turn on of the SCR along with SCR till the trigger pulse should be applied anode ct raises above the Latching Ct

Holding Ct: It is associated with turn off process. It is the min. Value of Ct below which Anode Ct should fall for the reliable turn off of the SCR

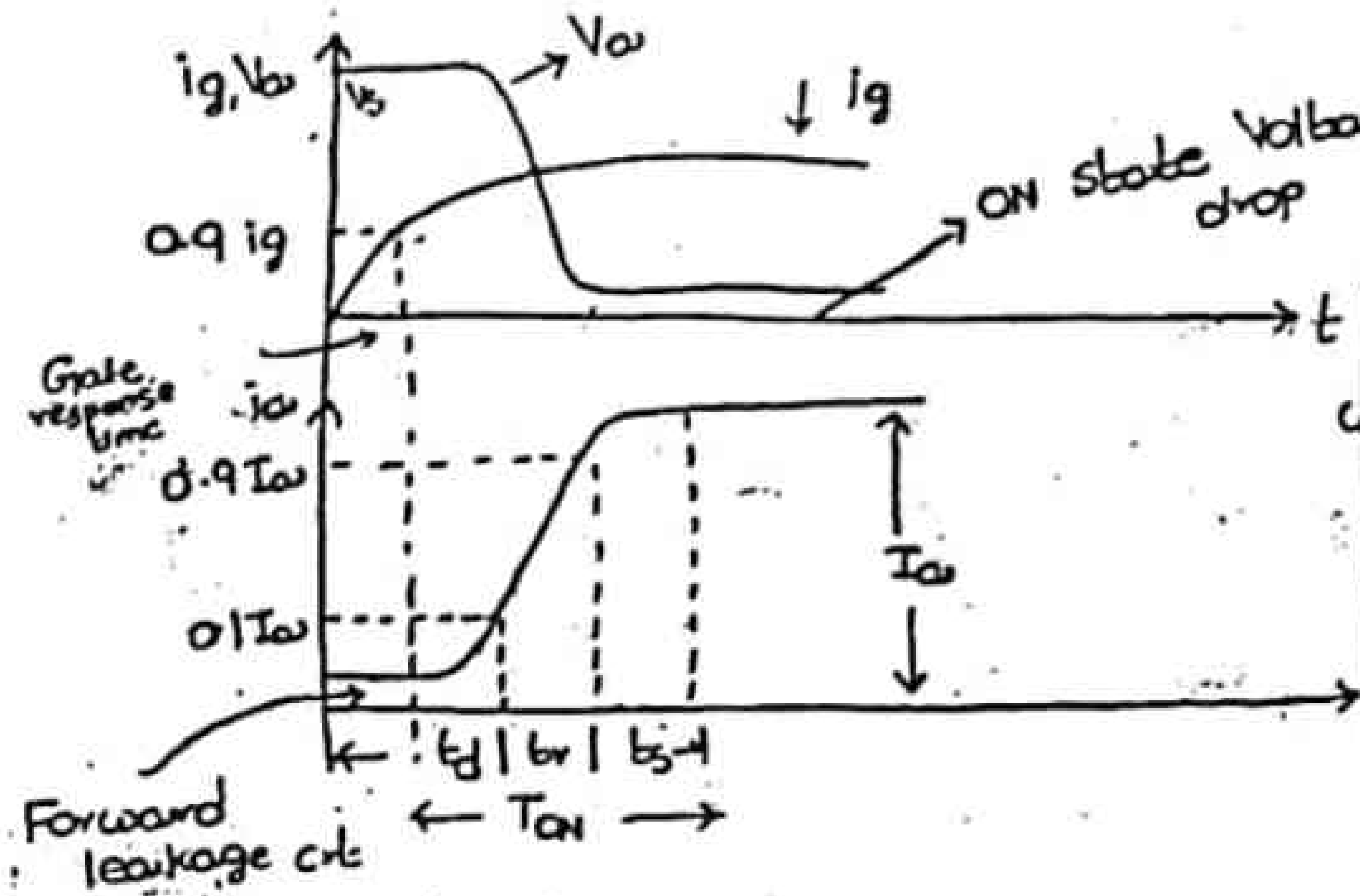
* It is useful to apply the reverse Voltage during turn-off process of the SCR

$\boxed{I_L > I_H}$ * $\boxed{\frac{I_L}{I_H} = 2.5-3}$

In reverse blocking state, J_1 & J_3 are reverse biased but J2 is forward biased and only reverse ... and allow the conduction in reverse direction is known as Reverse Break over Voltage

* SCR is having "higher reverse Voltage drops" and "power loss". So, it is not allowed to utilise in the "Reverse Conduction State".

Dynamic / Switching Characteristics :-



$T_{on} = t_d + t_r + t_s$
where t_d = delay time
$\Rightarrow (0.9\, I_g - 0.1 I_a)$
t_r = Rise time
$\Rightarrow 0.1 I_a - 0.9 I$
t_s = Spread time
$\Rightarrow 0.9\, I_a - I_a$.

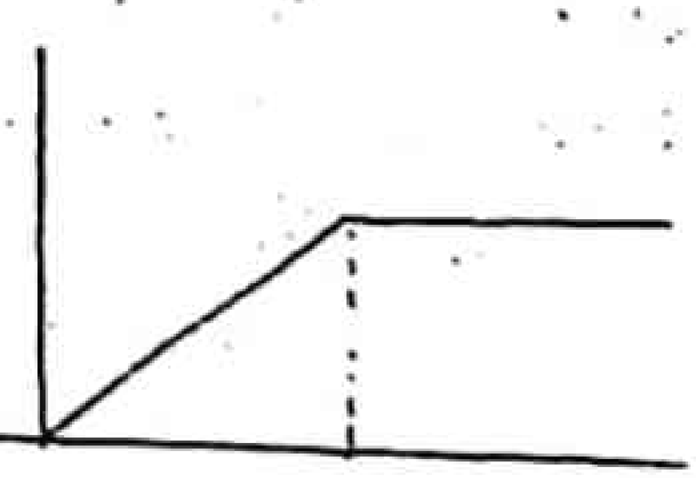
Turn on Time:- It is the time taken by the SCR from the instant of 0.9 Ig to steady state value of Anode Current (or Load Current)

* SCR is Considered to be charge Controlled device by employing higher values of Gate Current, turn on time Can be decreased.

Eg:- $Q = 1\,\mu C$
$Q = I \times t$
$1\,\mu C = 1A \times 1\,\mu s$
$= 2A \times 0.5\,\mu s$
$= 5A \times 0.2\,\mu s$

* "Higher Values" of "Gate Current" will "reduce" the "delay time"; it in turn "reduces" the "total turn on time".

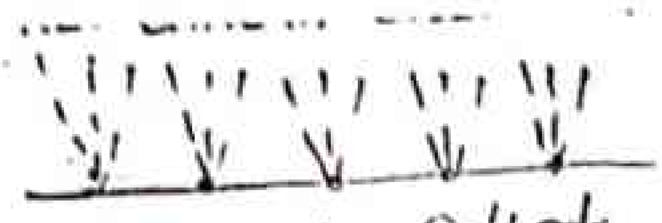
* During the turn-on process, local hot spots could be formed if rate of rise of Anode Current (di/dt) is more than the spreading Velocity of charge Carriers.



* This is due to non-Uniform Current distribution on the cathode surface.

* Local hot spots can be avoided by employing lower

* Local hot spots dominantly occur during rise time interval as the power loss is more in that duration



$\uparrow t_r \times t_1 \downarrow$ Spread (t_1)   Rise of I_a (t_2)

$(t_2 > t_1)$

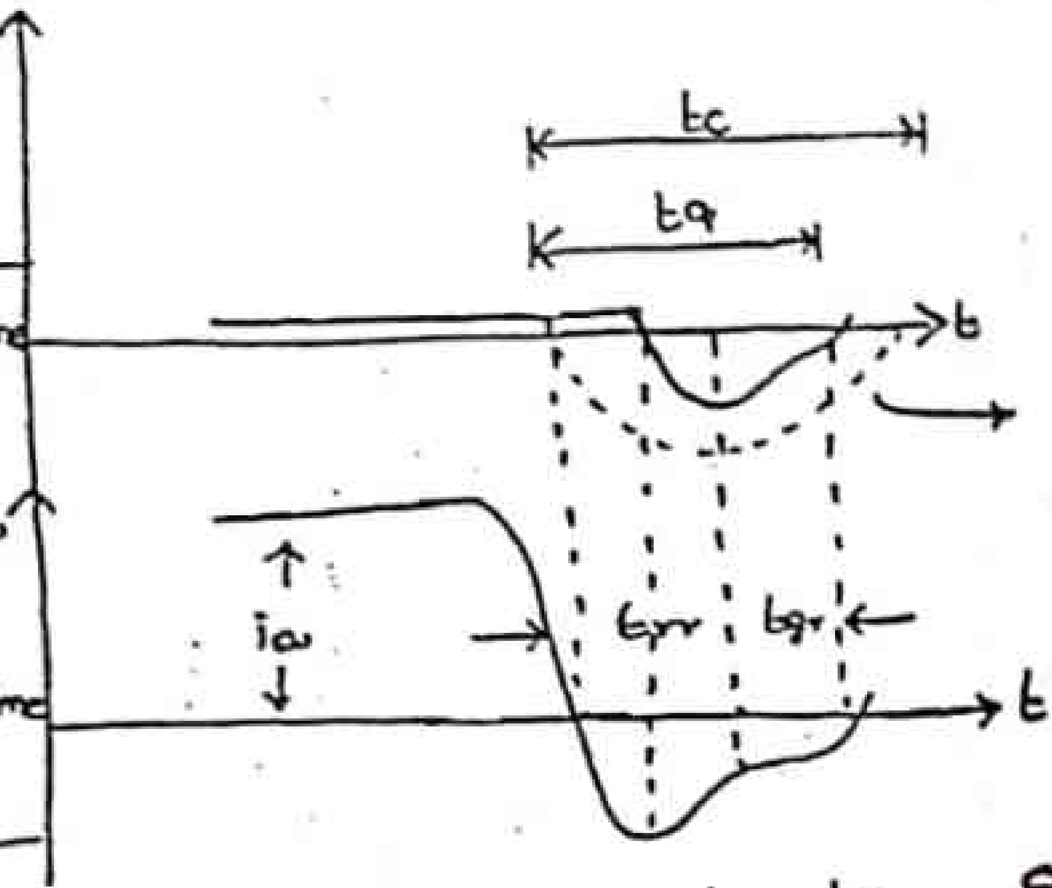
1 μs ✓   100 μs

100 μs ✗   1 μs

$\downarrow \frac{di}{dt} \times t_2 \uparrow$

25/4/12
6-8) pm

Turn - Off :-



t_q = Device turn off time

t_c = Ckt " "

$t_q = t_{rr} + t_{gr}$

Where t_{rr} = Reverse Recovery time

t_{gr} = Gate "

* The following conditions are to be satisfied for the turn-off of SCR

a) Reduce the Anode Current below Holding Current

b) Apply Reverse Voltage for sufficient duration to remove the energy possessed by charge carriers. It will be happened by removal of carriers. / by recombinations

A Special Circuit will be designed in Power Electronic Converters to apply the reverse voltage for the turn-off of the SCR. This Circuit is known as Commutation Circuit.

* Device turn off time:. It is the time reqd by the device to complete its turn-off process.

* Ckt turn off time:. It is the time given by the Ckt for the SCR to complete its turn-off process

Always $t_c > t_q$

* During the reverse recovery time, external layers will be recovered by removal of carriers.

* During gate recovery time, inner layers will be reco by recombinations

* SCRs with $t_q \leq 50$ μsec are known as

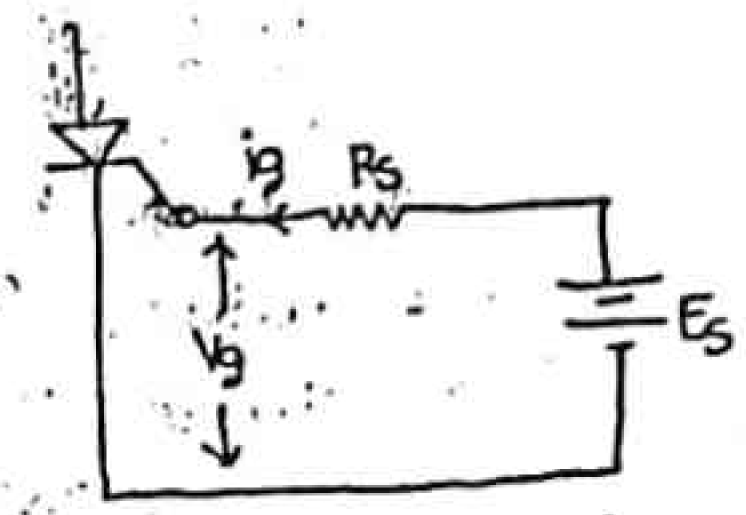
Eg:- Inverters, choppers & step up Cyclo Converters.

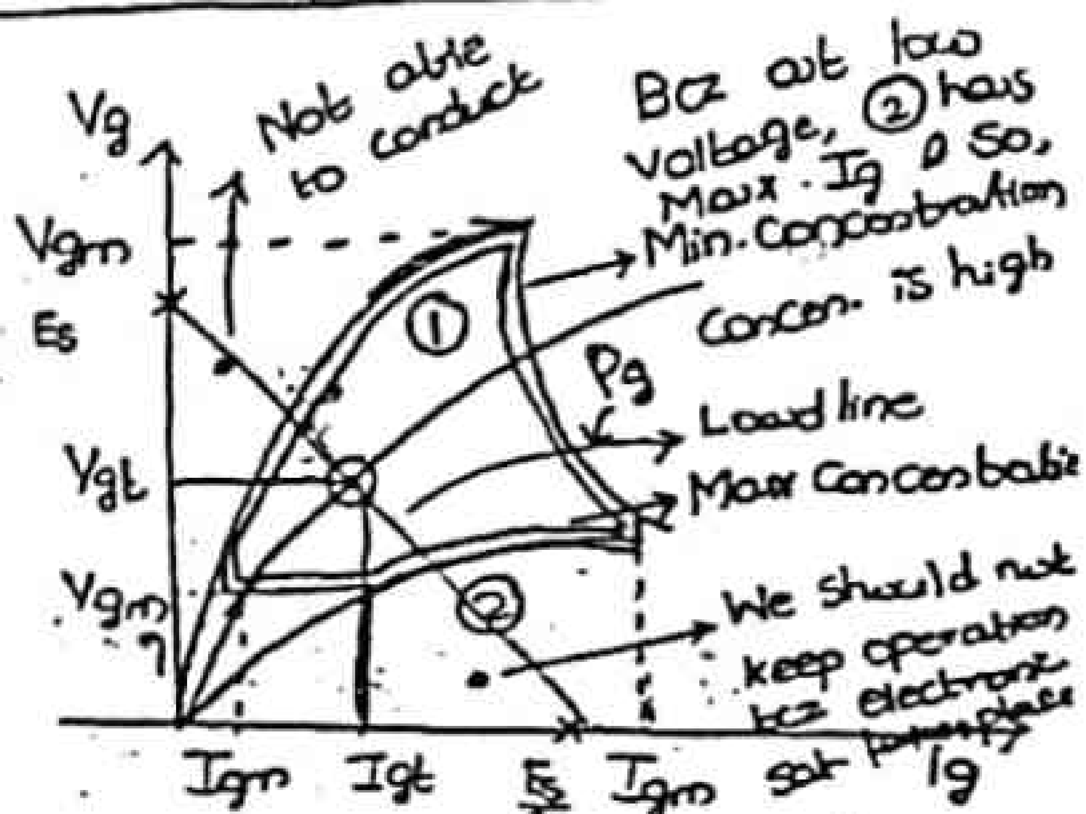
(*) SCR's with slow turn-off time ($t_q > 50\,\mu sec$) are known as Converter grade SCRS

Eg:- Appns:- phase Controlled rectifiers, Ac Voltage Controllers, step down Cyclo converters.

(*) If the temp. & Current through SCRS Increases then turn-off / device turn-off time also increases

Gate characteristics:-





* Gate characteristics of SCR is same as the forward characteristics of pn-Junction

* The min. Value prescription over the positioning of operating point is to over & avoid the Mal triggering due to noise signal

If $i_g = 0$, $V_g = E_s$ and If $V_g = 0$, then S.C occurs then max Current flows $i_g = E_s/R_s$

(*) Gate operating point :- V_{gt}, I_{gt} will be obtained by the intersection of Gate to cathode characteristics and load line.

* operating points should be so selected that the resultant gate currents are higher in Magnitude so that turn on time decreases.

$$\boxed{\begin{aligned} E_s &= V_g + i_g R_s \\ P_g &= V_g \cdot i_g \end{aligned}}$$

Slope of Gate to cathode characteristics $= \dfrac{V_g}{I_g}$ (V/A)

slope of Load line $= \dfrac{E_s}{\alpha} = R_s$

Protection of SCR :-

a) Over Voltage Protection - Varistor, Variable Capacitor

b) Over Current protection - Circuit breaker, Fuse, Fast acting Current limiting

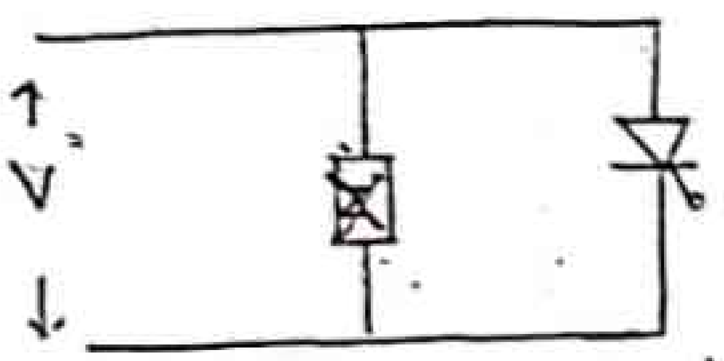
c) thermal protection - $\boxed{\text{Heat Sinks (Aluminium)}}$

d) dv/dt Protection - Snubber Ckt (Series R, C Combination)

e) dI/dt Protection - Series Inductor

* Voltage slowly increases but not suddenly, if it crosses 'Z' damages & SCR protect

a)



$V\uparrow \longrightarrow Z\downarrow \longrightarrow R\downarrow$

$\qquad\qquad\quad \longrightarrow X_C\downarrow \longrightarrow C\uparrow$

$V\downarrow \longrightarrow Z\uparrow \longrightarrow R\uparrow$

$\qquad\qquad\quad \longrightarrow X_C\uparrow \longrightarrow C\downarrow$

$V = L\frac{di}{dt}$

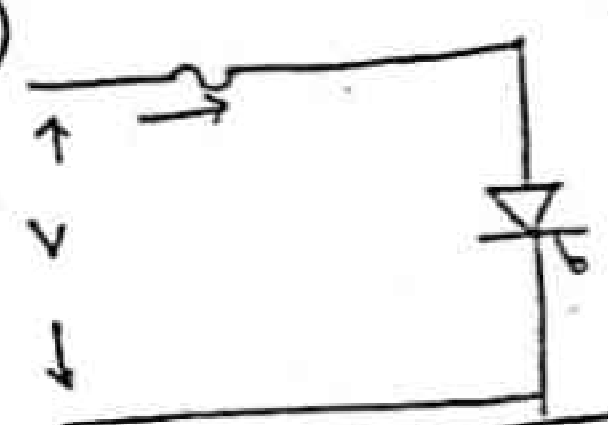
All loads are inductive in nature, so when there is change in current due to switching operation

$V = L\frac{di}{dt}$

$= L\frac{di}{0} = \infty$

So, over voltages occur

b)



* If high currents occur before circuit breaker trips, fuse will blow (Less time)

If over load occur the circuit breaker trips, If CB don't trip, fuse take more time to blow, device gets heated up

If normal fuses are used, then fuse is safe but SCR is damaged. But if Fast acting fuse (Semi Conductor) used SCR is protected

d) For safe operation, $\frac{dv}{dt}$ should be low. For getting low [dv/dt] there are two ways

1) dv should be low

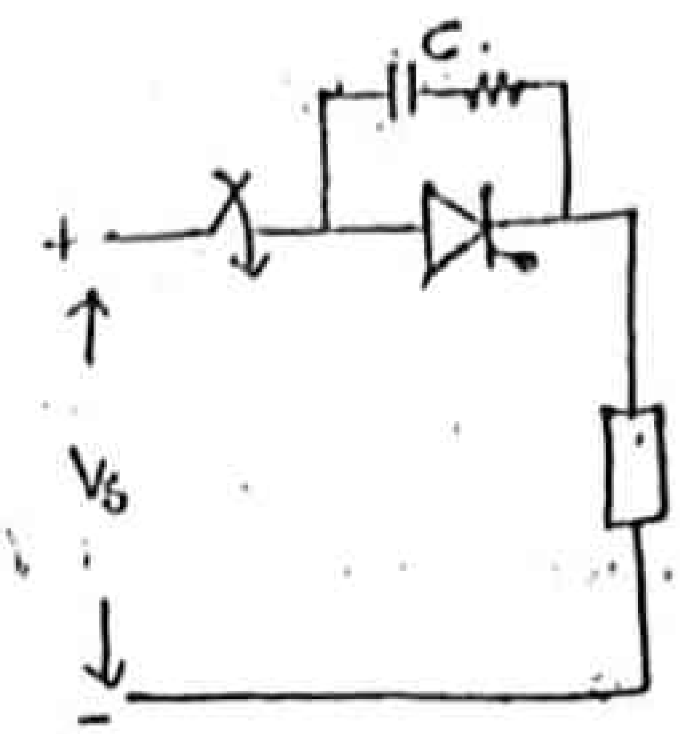
$V_1 = 0$
$V_2 = V_S$ $\quad\downarrow dv = V_S$
So, no possibility
bcz SCR is a swi

2) dt should be high

$\downarrow$

So, take little more time, th development of Voltage across SCR is delayed which can b Capacitor

26/4/12 (6p to 8p)



W/o Capacitor — With Capacitor :-

$V_1 = 0$ — $V_1 = 0$

$V_2 = V_S$ — $V_2 = V_S$

t_1 — t_2

$(t_2 > t_1)$ then $\frac{dv}{dt} \downarrow$

* Resistance in the Snubber Ckt is to limit the discharge the Current to Safe Value while the SCR Comes into Conduction.

e) $\frac{dI}{dt}$ protection :- $dI \downarrow$ (or) $dt \uparrow$

$\Downarrow$

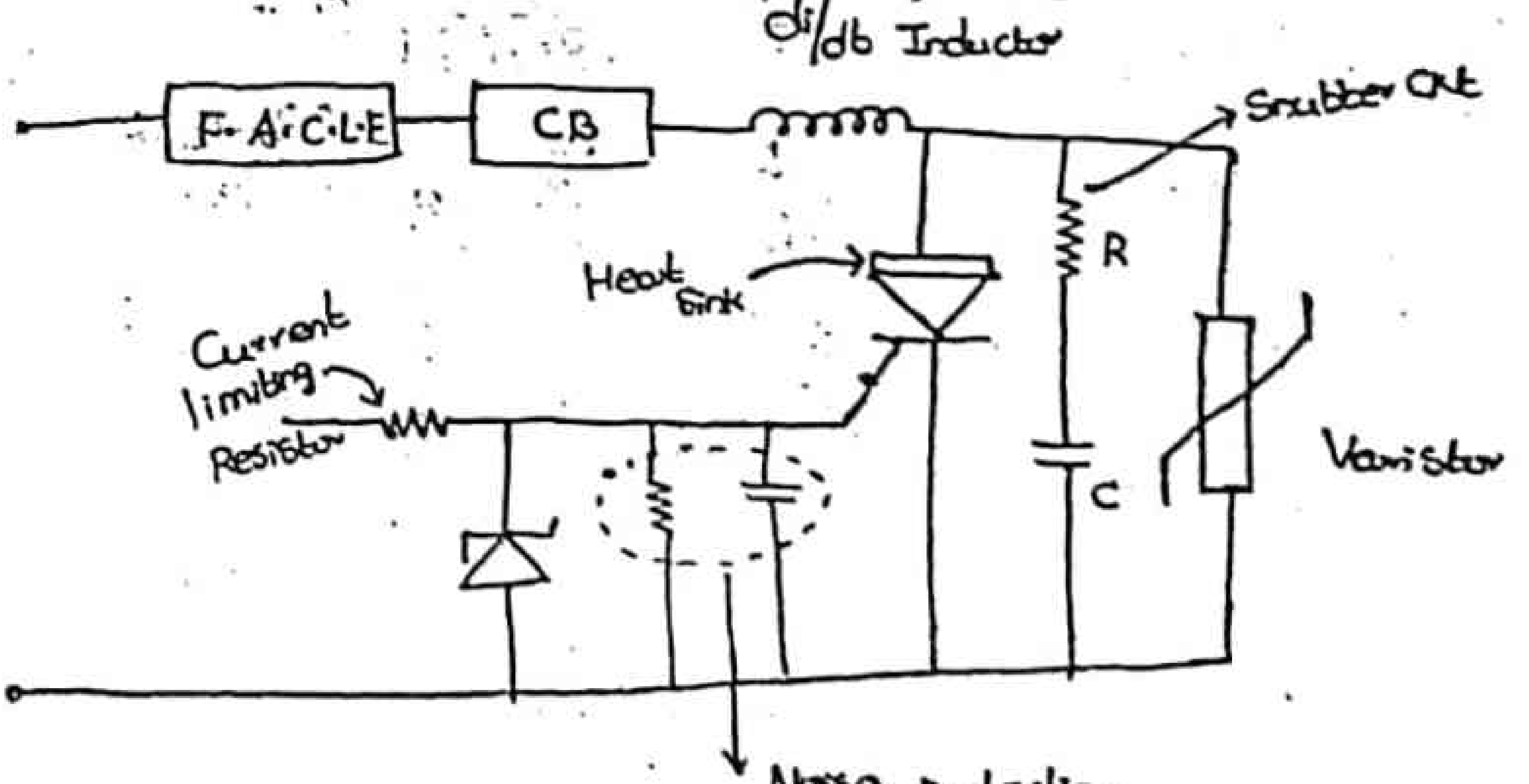
$I_1 = 0$

$I_2 = I_L$

$\downarrow dI = I_L \downarrow$

(We dont allow to decrease I_L because it merely depends on our requirement).

So, the only chance is to delay the SCR in building up the Current which could be possible only by an Inductor (So, it is used as Series Inductor)

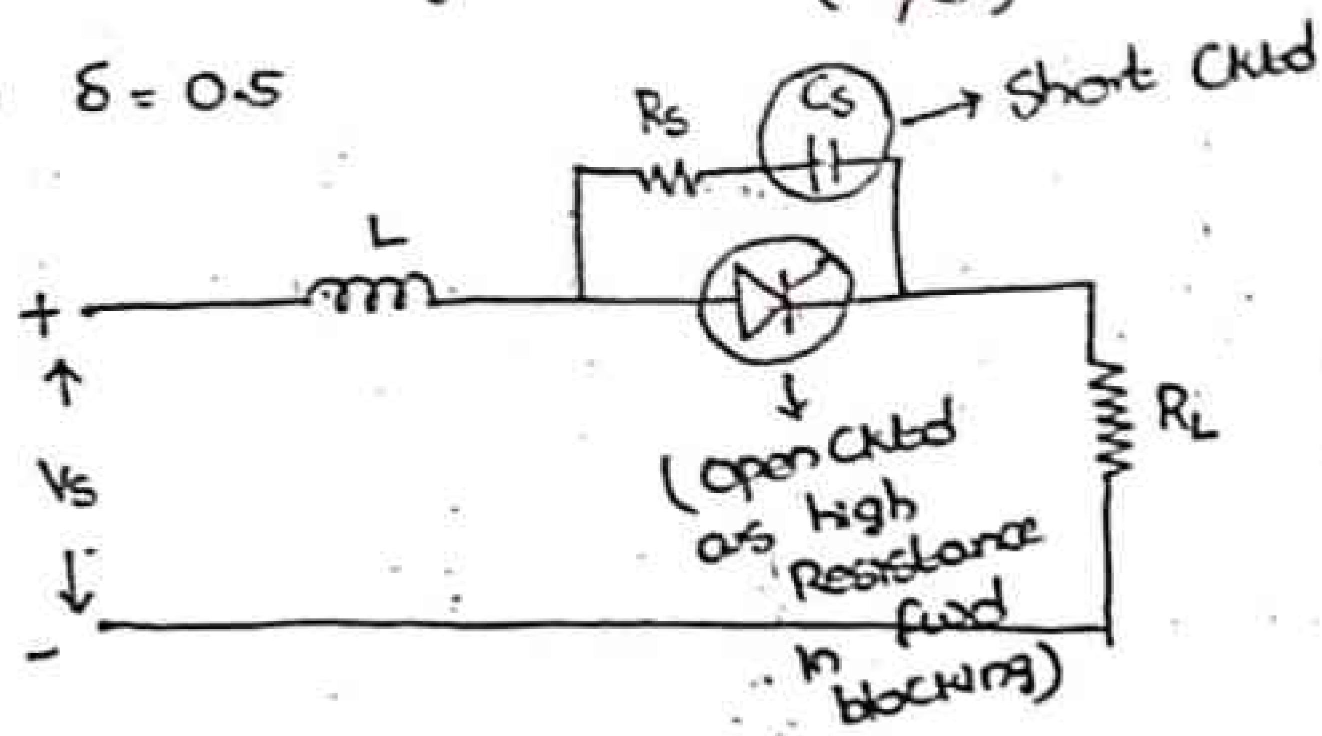


* A Resistance Connected across Gate to Cathode terminals is to make the protection against Noise Signals.

* Design of Snubber Ckt :

P. A Thyristor is placed b/w a Const. Dc Voltage Source of $V_s = 240$ V and a load Resistance of R_L. The Specified limits of (dv/dt) and (di/dt) of SCR are 300 V/μs & 60 A/μs respectively. Determine the Values of Snubber Ckt Parameters along with (di/dt) Inductor. Take damping Ratio $\delta = 0.5$

Inductor - open
Capacitor - Short



$$V_s = L\frac{di}{dt} + (R_s + R_L)\,i$$

$$\Rightarrow \frac{di}{dt} + \left(\frac{R_s+R_L}{L}\right) i = \frac{V_s}{L}$$

$$i = \frac{V_s}{(R_s+R_L)}\left[1 - e^{-\left(\frac{R_s+R_L}{L}\right)t}\right]$$

$$\Rightarrow \frac{di}{dt} = \frac{V_s}{(R_s+R_L)}\left\{0 + e^{-\left(\frac{R_s+R_L}{L}\right)t} \times \left(\frac{R_s+R_L}{L}\right.\right.$$

$$\frac{di}{dt} = \frac{V_s}{L}\, e^{-\left(\frac{R_s+R_L}{L}\right)t}$$

$$\left.\frac{di}{dt}\right|_{t=0} = \frac{V_s}{L} e^{-0} = \frac{V_s}{L}$$

$$\Rightarrow \boxed{L = \frac{V_s}{(di/dt)}}$$

$$V = i \cdot R_s$$

$$\Rightarrow \frac{dv}{dt} = \frac{di}{dt} \cdot R_s \Rightarrow \boxed{R_s = \frac{(dv/dt)}{(di/dt)}}$$

* In Series RLC ckt energised by DC Supply then KVL eqn becomes

* Series, Parallel Operation of SCRS:

* SCRS should be connected in series to get higher Voltage Ratings. SCRS should be connected in llel to get higher Current Ratings.

$$\eta_{str} = \left(\frac{\text{Actual Voltage rating of the String}}{\eta_s \times \text{Actual Voltage rating of each SCR}} \right)$$

(Series operation)

$$\eta_s = \left(\frac{\text{Actual Current rating of the string}}{\eta_p \times \text{Actual current rating of SCR}} \right)$$

(parallel)

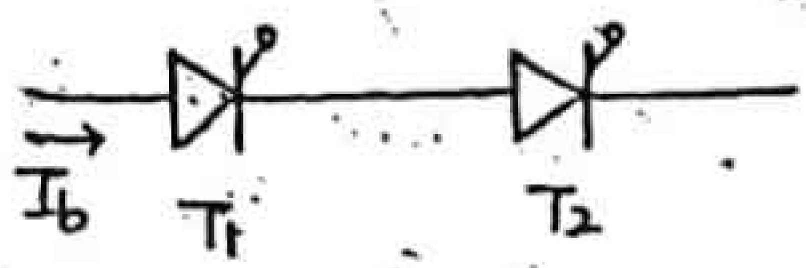
Always $\eta_s \leq 1$

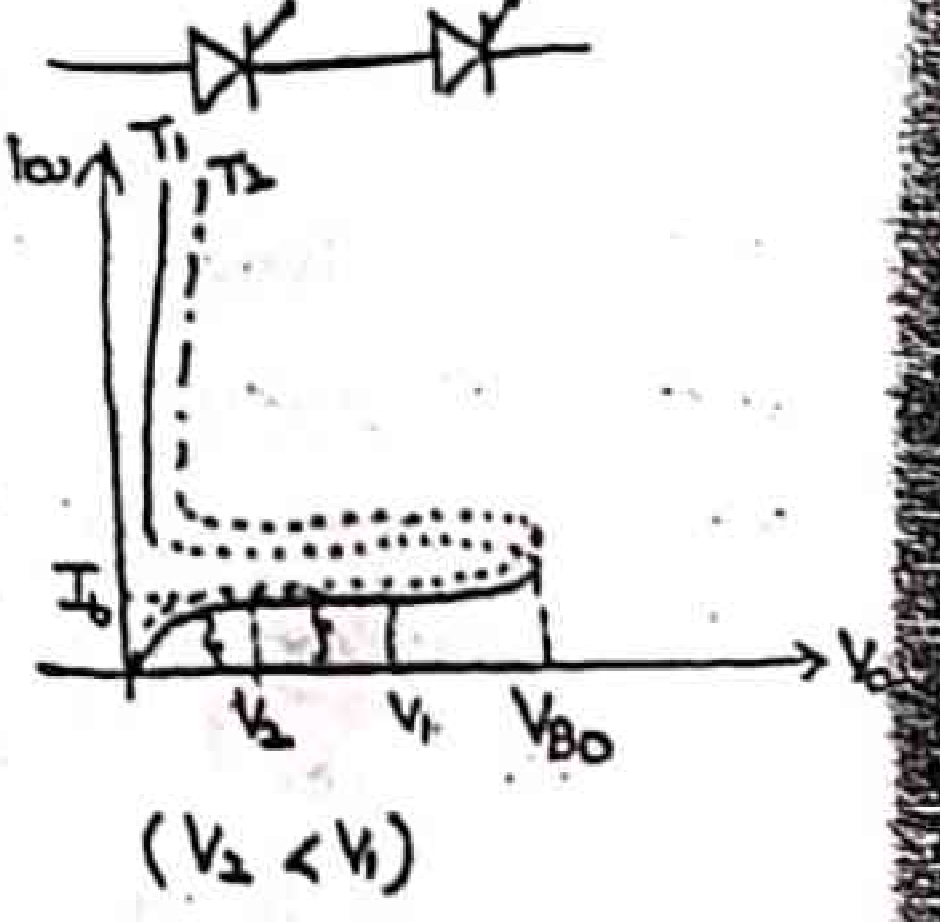
Derating factor (DRF) = $1 - \eta_s$

* Indicate Rating not useful to System performance

⊛ DRF physically denotes the rating of device which is not useful for the operation of the System. ⊛

Series operation of the SCRS:-





$(V_2 < V_1)$

$$\eta_s = \frac{V_1 + V_2}{2V_1}$$

$$= \frac{1}{2}\left(1 + \frac{V_2}{V_1}\right)$$

$$< 1$$

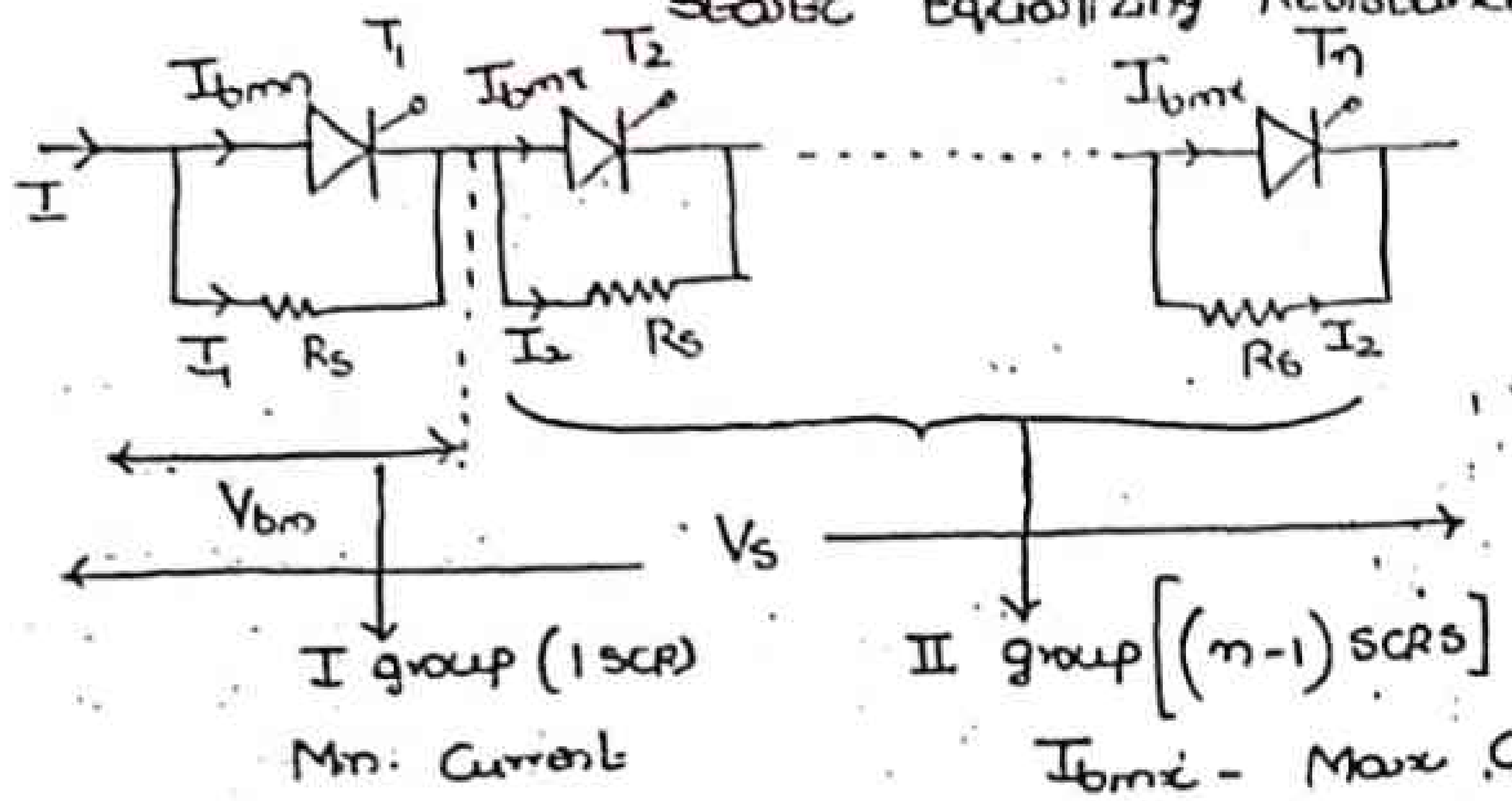
The unequal static characteristics results into unequal Voltage distribution among Series Connected SCRS

* The unequal voltage distribution is because of unequal leakage Resistances offered by SCRS. If the Resistance is more, it will block more Voltage ... the less leakage Current

* To Approximately equalize the Voltage distribution, it is proposed to connect only one Value of Resistance across each & every SCR and it is known as Static equalizing Resistance.

28/4/12 (9A 6(A))

Static Equalizing Resistance:



$I = I_1 + I_{bmn}$

$I = I_2 + I_{bmx}$

$$V_S = I_1 R_S + (n-1) I_2 R_S$$

$$= I_1 R_S + (n-1)\{I - I_{bmx}\} R_S$$

$$= I_1 R_S + (n-1)\{I_1 + I_{bmn} - I_{bmx}\} R_S$$

$$= I_1 R_S + (n-1)\{I_1 - (I_{bmx} - I_{bmn})\} R_S$$

$$= I_1 R_S + (n-1)\{I_1 - \Delta I_b\} R_S$$

$$= I_1 R_S + (n-1) I_1 R_S - (n-1) \Delta I_b R_S$$

$$= n I_1 R_S + (-1)(n-1) \Delta I_b R_S$$

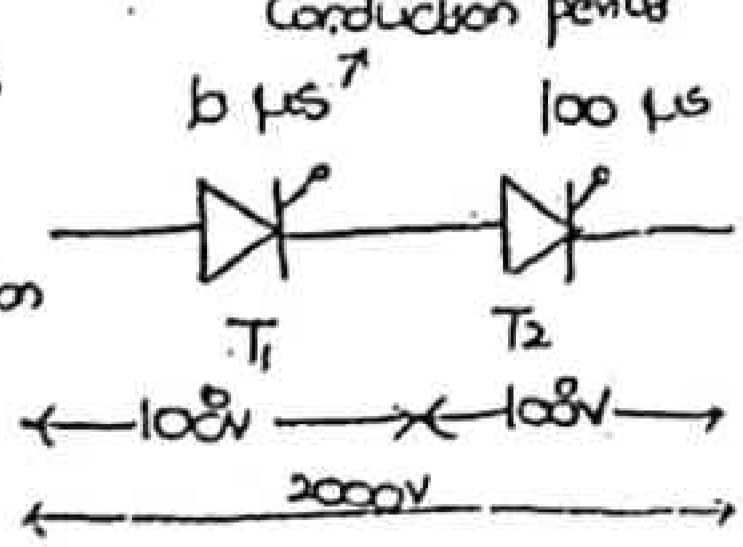
$$\Rightarrow V_S = n V_{bm} - (n-1) \Delta I_b R_S$$

$$\Rightarrow \boxed{R_S = \frac{n V_{bm} - V_S}{(n-1)\Delta I_b}}$$

ΔI_b = Diff. in leakage Current Ratings

* Dynamics properties:

* The unequal dynamic properties results into damage of the slower devices due to the application of excess Voltage

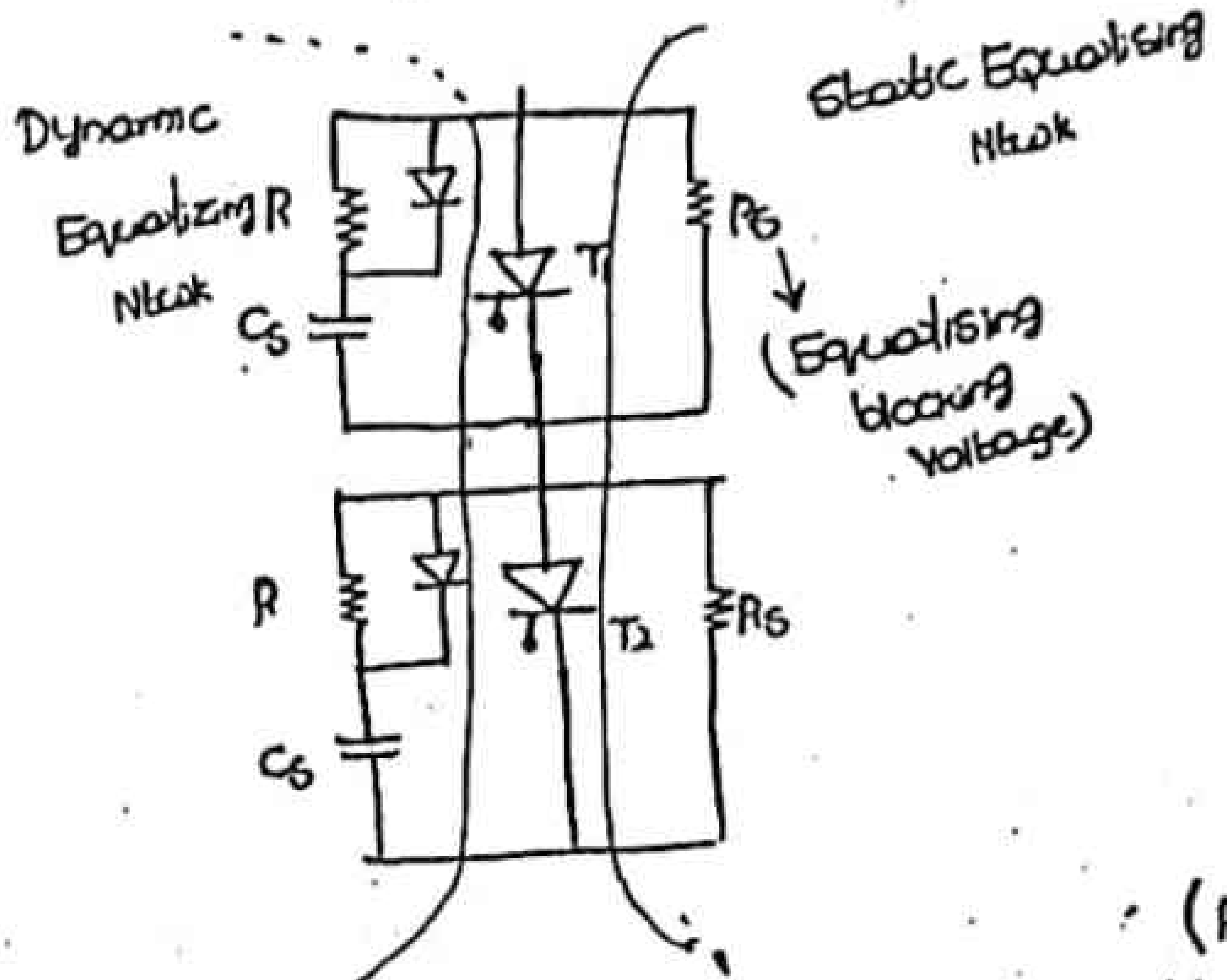


* Unequal Dynamic properties are due to unequal junction Capacitances

* Inorder to equalize the dynamic properties. It is proposed to connect one value of capacitance across each & every SCR and it is known as Dynamic Equalising Capacitance

$$\boxed{C = \frac{(n-1)\Delta Q}{n V_{bm} - V_s}}$$

ΔQ = Diff. in Reverse Recovery charge

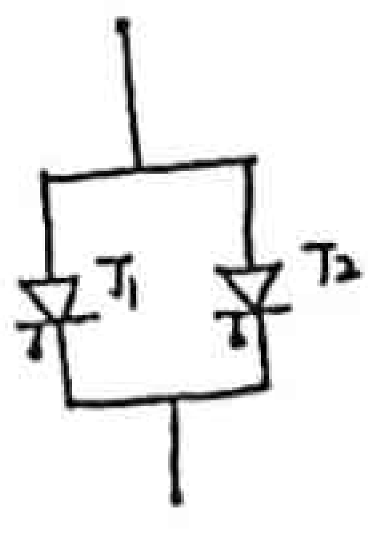


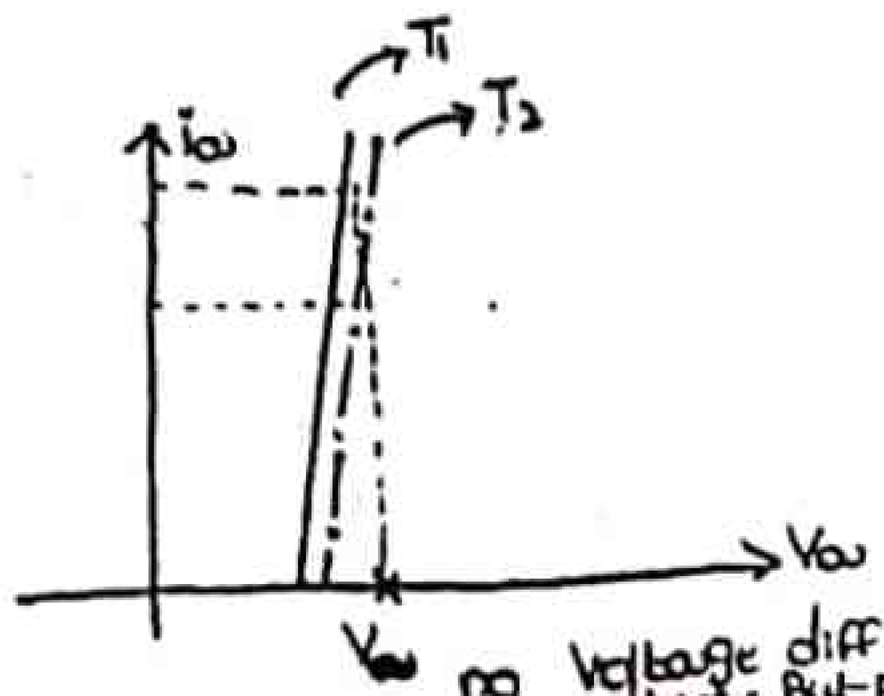
Capacitor should not be used alone, must be used along with a Resistor

* In the series operation, Snubber Circuit serves Dual purpose
  i) dv/dt protection
  ii) Dynamic properties Equalization

* Diode placed across Resistance will by pass the resistance while applying the forward voltage. It ensures the fast development of voltage across capacitor

Parallel operation:





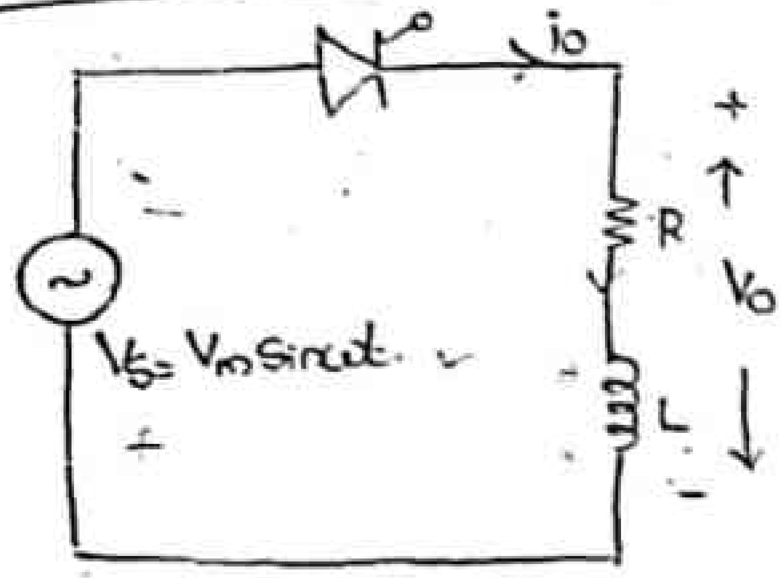
no voltage diff must be there. But practically some forward

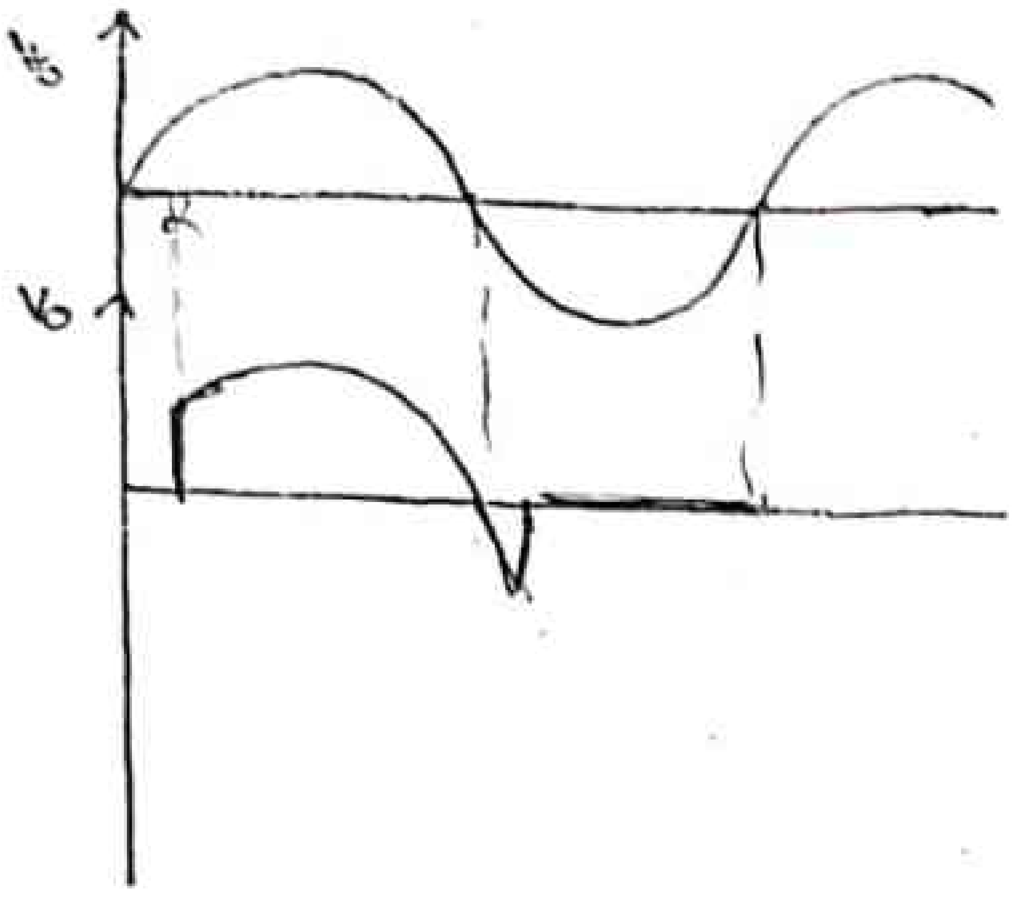
[Ideally T_1, T_2 'on' ⊗ on. state exists on each SCR as both SCRs are connected in ||el - So, consider it as 'V_a']

$$\eta_s = \frac{I_1 + I_2}{2 I_1} < 1$$

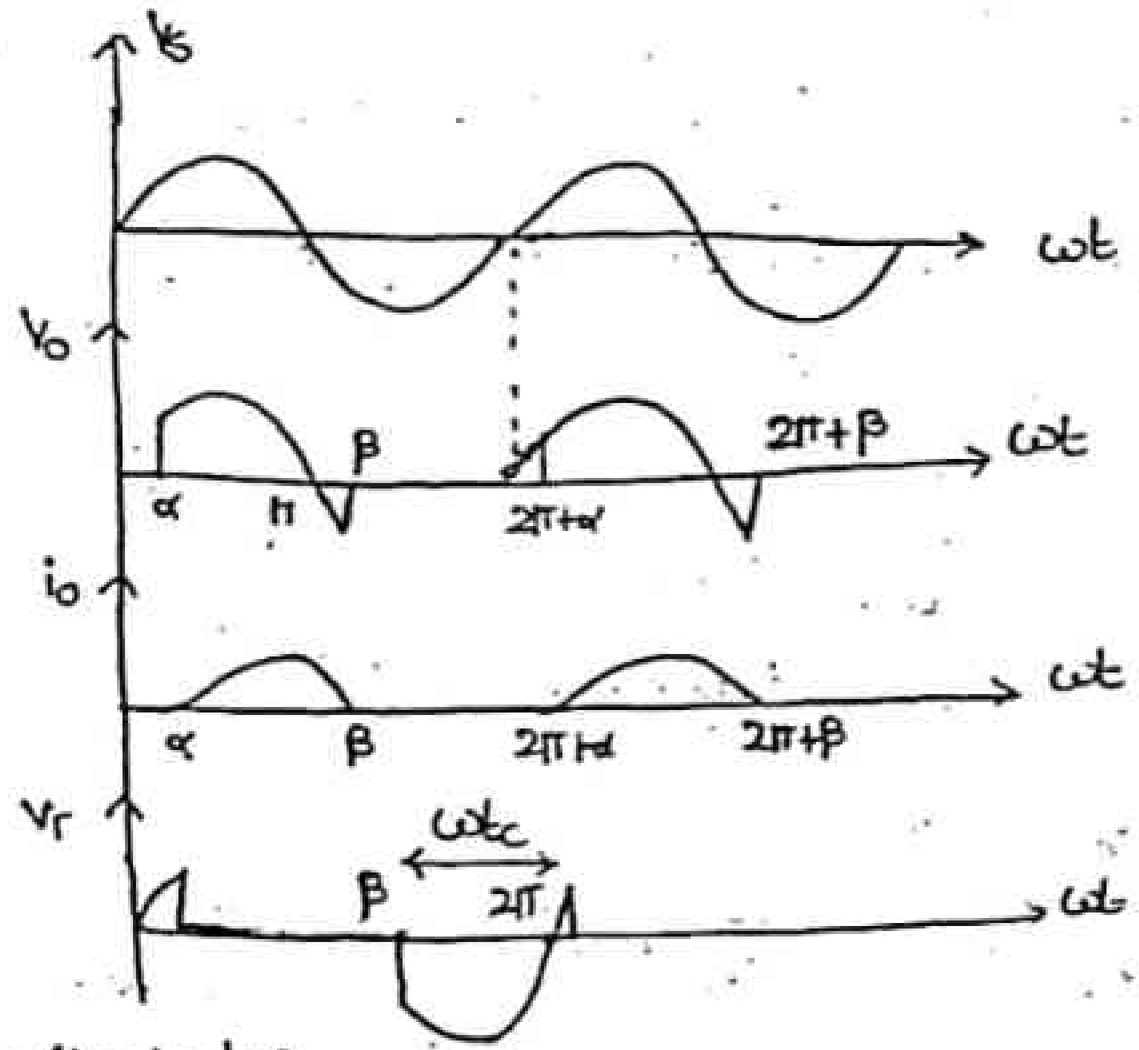
30/1/12.
(6 to 8:30)

1-ϕ Half Wave RL Load:-





* In the case of R-L Loads, $\beta > \pi$. Whereas in the case of R- Load, $\beta = \pi$.



* In this ckt, turn off time is $\omega t_c = 2\pi - \beta$

$$\boxed{t_c = \frac{2\pi - \beta}{\omega} \text{ sec}}$$

Avg. Value

$$V_o = \frac{1}{2\pi}\int_\alpha^\beta V_m \sin\omega t \, d(\omega t)$$

$$= \frac{V_m}{2\pi}\left(-\cos\omega t\right)_\alpha^\beta$$

$$\boxed{V_o = \frac{V_m}{2\pi}\left(-\cos\beta + \cos\alpha\right)}$$

$$V_{or} = \sqrt{\frac{1}{2\pi}\int_\alpha^\beta \left(V_m^2 \sin^2\omega t \, d\omega t\right)}$$

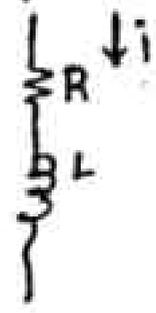
$$V_{or}^2 = \frac{V_m^2}{2\pi}\int_\alpha^\beta \left(\frac{1-\cos 2\omega t}{2}\right) d\omega t$$

$$= \frac{V_m^2}{4\pi}\left(\omega t - \frac{1}{2}\sin 2\omega t\right)_\alpha^\beta$$

$$= \frac{V_m^2}{4\pi}\left(\beta - \alpha + \frac{1}{2}\sin(2\alpha - \sin 2\beta)\right)^{1/2}$$

$$\boxed{V_{or} = \frac{V_m}{2\sqrt{\pi}}\left((\beta-\alpha) + \frac{1}{2}\left(\sin(2\alpha) - \sin 2\beta\right)\right)}$$

$Z = R + jX_L = R + j(2\pi f)L$



Here it is not Cyclic in nature, so ∠-1
(or) Another Reason is the effect of inductor is not taken because the avg. Value of inductor voltage is zero

$$\frac{\bigcirc = 0}{\bigcirc}$$

Input Supply P.f = $\dfrac{\text{Power delivered to load}}{\text{Source VA}}$

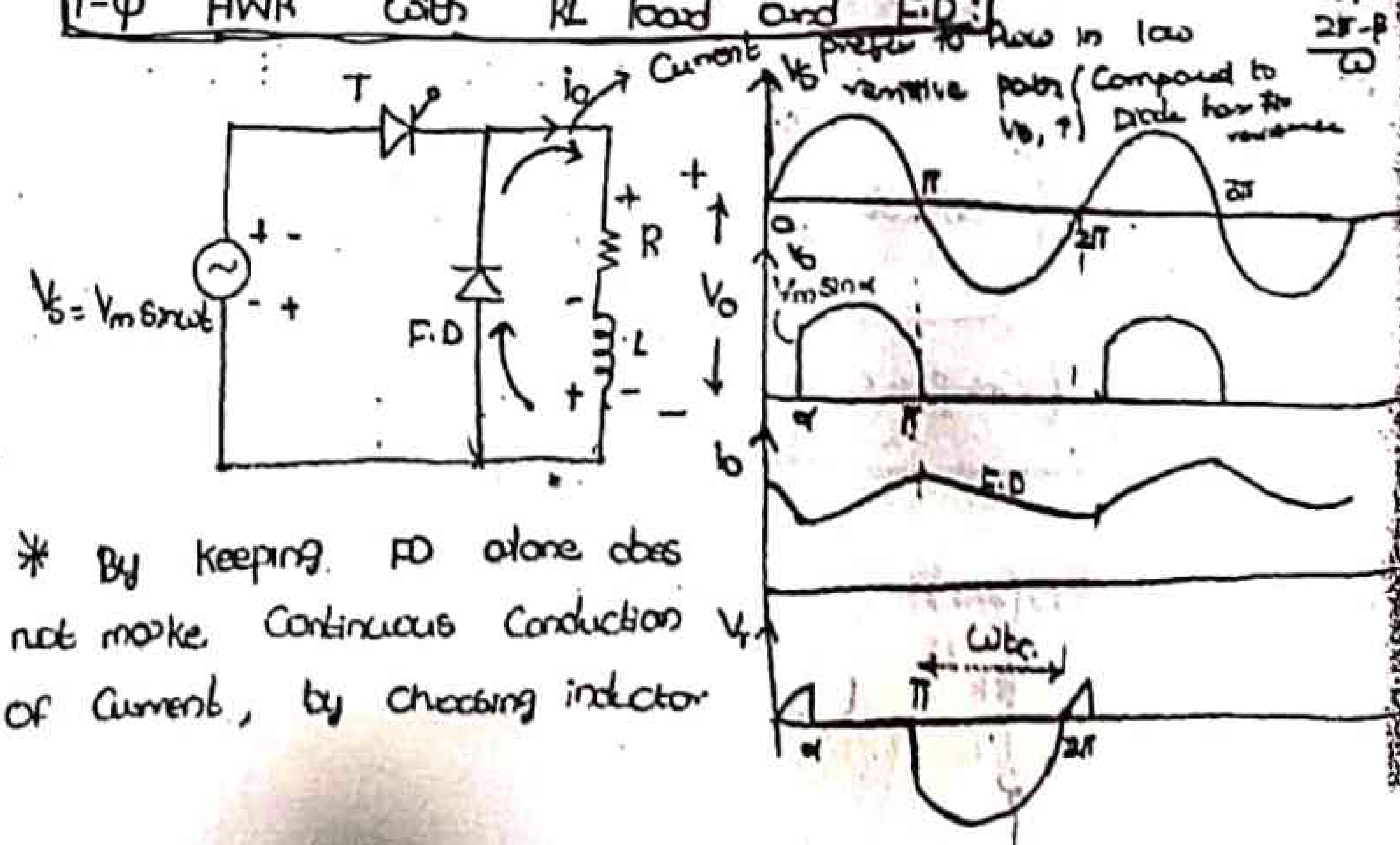
$$= \frac{V_{or}^2/R}{V_s \cdot I_{sr}} = \frac{V_{or}^2/R}{V_s \cdot V_{or}/R}$$

$$\Rightarrow \boxed{PF = \frac{V_{or}}{V_s}}$$

* During α to π, Power is +ve ; π to β power is Negative. The avg. power Consumption is decreased. (or in other words) Rated power will not be Consumed by the load.
* To Stop the power flow from Load to Source, a diode will be Connected across the load terminals and it is known as Free-Wheeling diode
* Ckt turn-off time is less than $\frac{\pi}{\omega}$ and it is of Variable (Because always $\beta > \pi$ So, $t_c = \frac{2\pi-\beta}{\omega}$)

1-φ HWR with RL load and F.D:

Current prefer to flow in low resistive path (Compared to V_s, T) Diode has the resistance



* By keeping FD alone does not make Continuous Conduction of Current, by Choosing inductor

$\omega t_c = \pi$

$\Rightarrow \boxed{t_c = \frac{\pi}{\omega} \text{ sec}}$

Ckt turn off time is w.r.t SCR

* ADVANTAGES OF F.D :

a) Avg. Power Consumption is Increased.

b) Power factor also Improves

c) Ckt turn-Off time is equal to π/ω and it is of Constant Value

d) Chance of getting Continuous Conduction increased by keeping of F.D. It is possible if the Inductor is able to support Conduction from π to $2\pi+\alpha$.

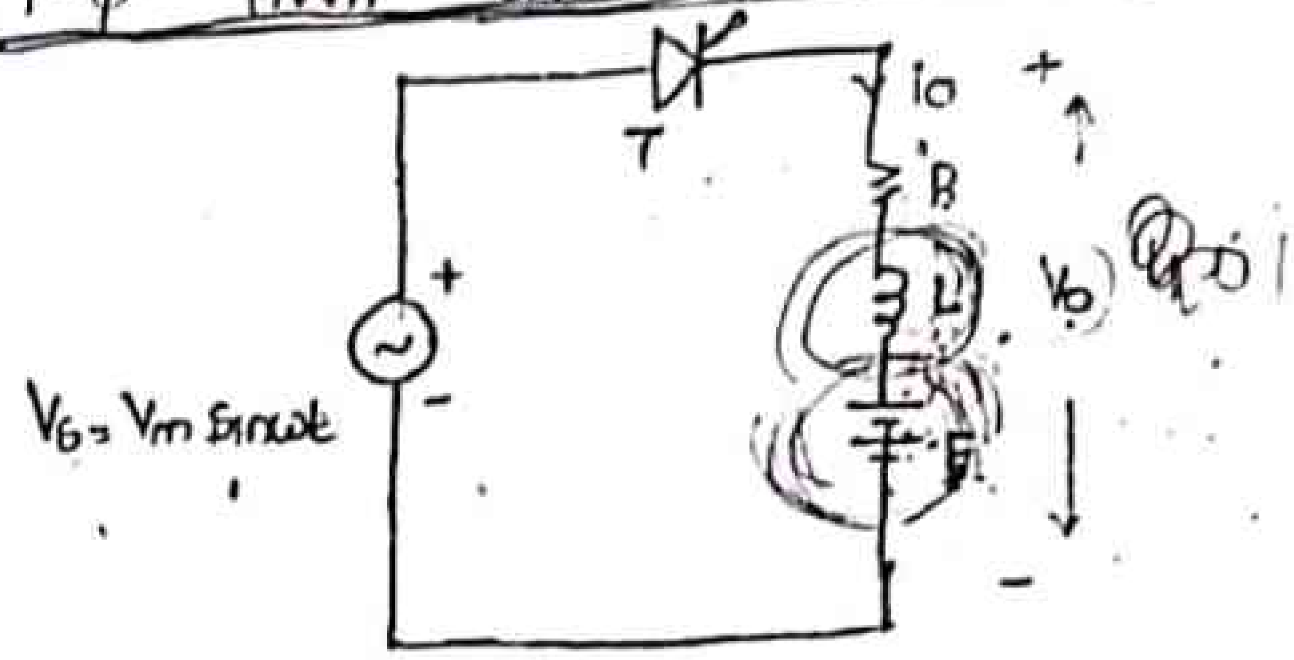
$$\boxed{\begin{aligned} V_o &= \frac{V_m}{2\pi}(1+\cos\alpha) \quad \text{(Same as R-Load)} \\ V_{or} &= \frac{V_m}{2\sqrt{\pi}}\left[\pi-\alpha+\frac{1}{2}\sin 2\alpha\right]^{1/2} \\ I_o &= \frac{V_o}{R} \\ I_{or} &= \frac{V_{or}}{R} \\ P_f &= \frac{V_{or}}{V_s} \end{aligned}}$$

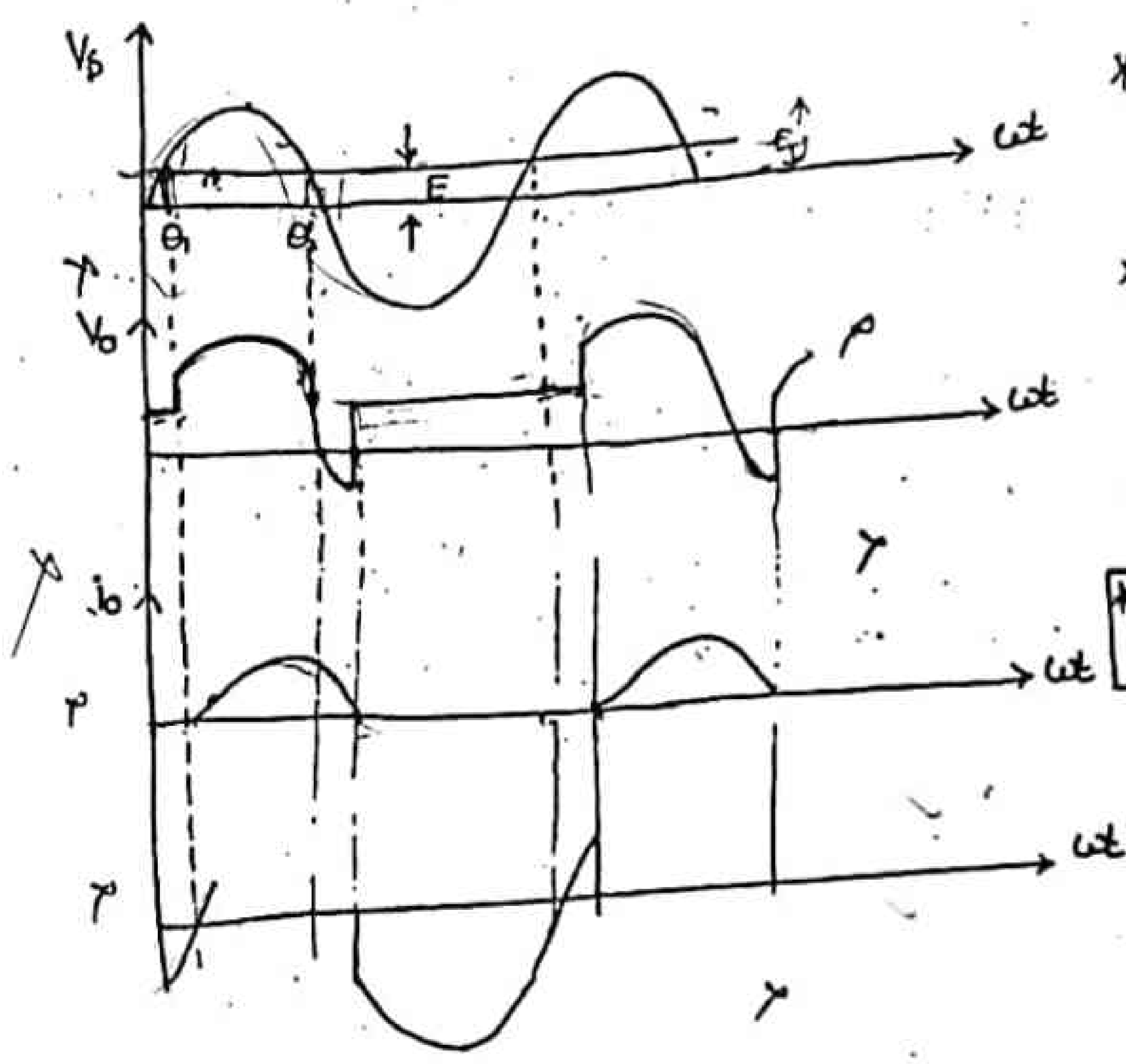
* The Continuous Current is Obtained based upon the Capacity of Inductor but on the FD. Even If the Capacity is less, though we have FD 'i' = 0

* o/p Voltage is zero bcz FD short Circuits load. Load does not Consume power.
power will be zero because (During FD Action)

* F.D Circulates the Current w/o taking any power from supply lines. So, it is known as F.D

1-φ HWR with RLE load:





* Unless $V_s >$ E, Thyristor is not F.B
* Up to θ_1, $V_s <$ E, it is reverse biased
* Up to θ_2, only it is F.B

$\boxed{\text{* Range of firing angle is } \theta_1 - \theta_2}$